REMARKS

The present application was filed on June 8, 2000 with claims 1-20. Claims 1-20 remain pending. Claims 1, 6, 13, and 20 are independent claims.

In the outstanding final Office Action dated July 2, 2004, the Examiner: (i) objected to the drawings; (ii) objected to claim 18; (iii) rejected claim 1 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,905,667 to Lee (hereinafter "Lee"); (iv) rejected claim 1 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 3,646,332 to Suzuki (hereinafter "Suzuki") in view of Lee; and (v) rejected claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,943,251 to Jiang et al. (hereinafter "Jiang") in view of Lee.

Applicant acknowledges the indication of allowable subject matter in claims 2-5. Claims 10 and 17 were not addressed in the final Office Action.

With regard to the objection to the drawings, the expression S(n) provided by the Examiner in the final Office Action in relation to claim 2, is functionally equivalent to structure of logic illustrated in FIG. 1. More specifically, the equivalence is proven using DeMorgan's Law, as explained in the previous response. Thus, ^[{p(n)*C(n-1)}+^{p(n)+C(n-1)}] = ^{p(n)*C(n-1)}*{p(n)+C(n-1)}. Furthermore, FIG. 1 is supported by the text as set forth on page 3 of the specification and claim 2. Accordingly, withdrawal of the objection to the drawings is therefore respectfully requested.

With regard to the objection to claim 18, the claim was amended to include a period at its end.

With regard to the rejection of claim 1 under 35 U.S.C. §102(b) as being anticipated by Lee, Applicant asserts that such claims are patentable for the reasons presented below.

Lee discloses an adder that includes a static logic block, a first dynamic inverter logic block, a dynamic logic block, and a second dynamic inverter logic block for generating a sum through a sum output node. Lee further describes a dynamic logic version of an adder gate that uses a combination of inverting clock signals and short circuit current paths to conditionally discharge a dynamic node. This solution consumes excess power through the dc current path of the pullup device MN5 and MN71 in FIG. 5, with the pull-down trees. Lee also uses clock CLK and inverted

clock CLKB to prevent a pre-discharge of the dynamic node NODE52. The outputs SUM and CARRY can be in a high-impedance floating state when CLK is low and neither the SUM or CARRY is evaluated at a HIGH signal. This creates a noise sensitivity problem.

Independent claim 1 of the present invention recites a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. FIGS. 1-3 of Lee disclose conventional adder circuits and fail to disclose an adder circuit having dynamic logic, since no clock signals are used as input. Further, FIGS. 4 and 5 of Lee both use inverted clock signal CLKB to drive one or more dynamic nodes. In FIG. 4, inverted clock CLKB drives dynamic inversion gates 42 and 44, each of which comprises dynamic nodes. In FIG. 5, inverted clock CLKB drives dynamic node NODE52.

In response to arguments previously submitted by Applicant, the Examiner contends that FIG. 4 of Lee does not disclose any inversion signal of clock CLKB, which drives the dynamic nodes and is directly applied to the P-MOS and N-MOS transistors. However, in describing FIG. 4 in the specification of Lee (column 2, line 26 through column 3, line 43), CLK is referred to as the clock while CLKB is referred to as the inverted clock. Therefore, CLKB is, itself, an inversion of clock signal CLK. While a specific inverter is not shown in FIG. 4, it is clearly apparent from the disclosure of Lee that inverted clock signal CLKB is an inversion of clock signal CLK. Thus, since CLKB is an inversion of signal CLK which drives one or more dynamic nodes (e.g., NODE52), Applicant asserts that the circuit disclosed in Lee is distinguishable from the claimed invention.

Therefore, Lee fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. Accordingly, withdrawal of the rejection to claims 1 and 3-5 under 35 U.S.C. §102(b) is therefore respectfully requested.

With regard to the rejection of claim 1 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Lee, Applicant asserts that the Examiner has failed to set forth a proper *prima facie* case of obviousness as set forth in M.P.E.P. §2143.

Three requirements must be met to establish a *prima facie* case of obviousness. First, there must be some suggestion or motivation to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited combination must teach or suggest all the claim limitations. While it is sufficient to show that a *prima facie* case of obviousness has not been

established by showing that one of the requirements has not been met, Applicant respectfully believes that none of the requirements have been met.

First, there is clear lack of motivation to combine the references. Applicant asserts that no motivation or suggestion exists to combine Suzuki and Lee in a manner proposed by the Examiner, or to modify their teachings to meet the claim limitations. For at least this reason, a *prima facie* case of obviousness has not been established. Applicant strongly believes that one ordinarily skilled in the art would not look to Lee's dynamic logic blocks of a full adder to modify Suzuki's non-dynamic logical operation circuit device. That is, the teachings in the references are directed to completely different circuit topologies; a first (Lee) toward a dynamic adder, and a second (Suzuki) toward a non-dynamic adder. However, other than a very general and conclusory statement in the final Office Action, there is nothing in the three references that reasonably suggests why one would actually combine the teachings of these two references.

The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Lee, 277, F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344.

In the final Office Action at page 5, the Examiner provides the following statement to prove motivation to combine Suzuki and Lee, with emphasis supplied:

> [I]t would have been obvious . . . to use the dynamic logic as disclosed in Lee's invention into Suzuki's invention because it would enable to reduce the power consumption and increase the system performance.

Applicant submits that these statements are based on the type of "subjective belief and unknown authority" that the Federal Circuit has indicated provides insufficient support for an obviousness rejection. More specifically, the Examiner fails to identify any objective evidence of record which supports the proposed combination.

Second, with respect to claim 1, even assuming, *arguendo*, that the Suzuki and Lee references can be combined, Applicant asserts that there is no reasonable expectation of success in achieving the present invention through a combination of Suzuki and Lee absent the teachings of the present invention. For at least this reason, a *prima facie* case of obviousness has not been established. Despite the assertion in the final Office Action, Applicant does not believe that Suzuki and Lee are combinable since it is not clear to one skilled in the art how one would combine the two differing circuit architectures. There is no guidance provided in the final Office Action to support such a combination. However, even if combined, they would not achieve the unique teachings of the claimed invention.

Third, Applicant asserts that even if combined, the Suzuki and Lee references, when considered either individually or in combination, fail to teach or suggest all of the limitations of claim 1. For at least this reason, a *prima facie* case of obviousness has not been established.

Independent claim 1 recites that dynamic logic is provided without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. As acknowledged by the Examiner, Suzuki does not disclose dynamic logic. Thus, while Suzuki is non-analogous art, Lee fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic, as described above. Therefore, the combination of Suzuki and Lee also fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic.

Accordingly, withdrawal of the rejection to claim 1 under 35 U.S.C. §103(a) is therefore respectfully requested.

With regard to the rejection of claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) as being unpatentable over Jiang in view of Lee, Applicant asserts that the Examiner has failed to set forth a proper *prima facie* case of obviousness as set forth in M.P.E.P. §2143.

First, there is clear lack of motivation to combine the references. Applicant asserts that no motivation or suggestion exists to combine Jiang and Lee in a manner proposed by the Examiner, or to modify their teachings to meet the claim limitations. For at least this reason, a *prima facie* case of obviousness has not been established. Applicant strongly believes that one ordinarily skilled in the art would not look to Lee's dynamic logic blocks of a full adder to modify Jiang's non-dynamic

adder capable of handling multiple data of different types. That is, the teachings in the references are directed to completely different circuit topologies; one (Lee) toward a dynamic adder, the other (Jiang) toward a non-dynamic adder. However, other than a very general and conclusory statement in the final Office Action, there is nothing in the three references that reasonably suggests why one would actually combine the teachings of these two references.

In the final Office Action at page 6, the Examiner provides the following statement to prove motivation to combine Jiang and Lee, with emphasis supplied:

> [I]t would have been obvious . . . to use the dynamic logic as disclosed in Lee's invention into Jiang's invention because it would enable to reduce the power consumption and increase the system performance.

Applicant submits that these statements are based on the type of "subjective belief and unknown authority" that the Federal Circuit has indicated provides insufficient support for an obviousness rejection. More specifically, the Examiner fails to identify any objective evidence of record which supports the proposed combination.

Second, with respect to claims 6-9, 11-16 and 18-20, even assuming, *arguendo*, that the Jiang and Lee references can be combined, Applicant asserts that there is no reasonable expectation of success in achieving the present invention through a combination of Jiang and Lee absent the teachings of the present invention. For at least this reason, a *prima facie* case of obviousness has not been established. Despite the assertion in the final Office Action, Applicant does not believe that Jiang and Lee are combinable since it is not clear to one skilled in the art how one would combine the two differing circuit architectures. There is no guidance provided in the final Office Action. However, even if combined, they would not achieve the unique teachings of the claimed invention.

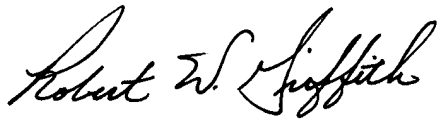
Third, Applicant asserts that even if combined, the Jiang and Lee references, when considered either individually or in combination, fail to teach or suggest all of the limitations of claims 6-9, 11-16 and 18-20. For at least this reason, a *prima facie* case of obviousness has not been established.

Independent claims 6, 13 and 20 recite that dynamic logic is provided without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. As acknowledged by the Examiner, Jiang does not disclose dynamic logic. Thus, while Jiang is non-analogous art, Lee fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic, as described above. Therefore, the combination of Jiang and Lee also fails to disclose a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic.

Dependent claims 7-9, 12, 14-16, 18 and 19 are patentable by virtue of their dependence on independent claims 6 and 13. Dependent claims 7-9, 12, 14-16, 18 and 19 also recite patentable subject matter in their own right. Accordingly, withdrawal of the rejection of claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) is therefore respectfully requested.

In view of the above, Applicant believes that claims 1-20 are in condition for allowance, and respectfully request withdrawal of the §102(b) and §103(a) rejections.

Respectfully submitted,



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